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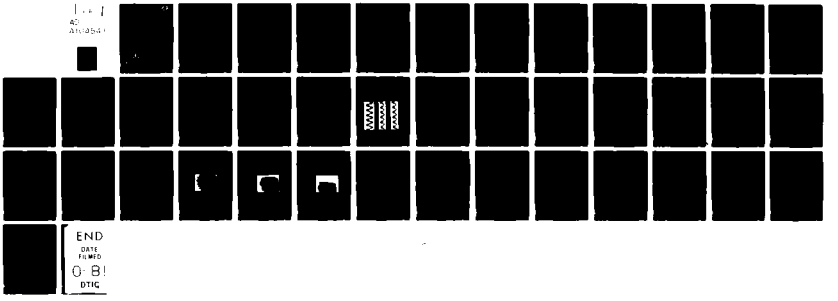

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THE CROSSTIE RANDOM ACCESS MEMORY (CRAM) PART 1 – THE CONCEPT AND INITIAL STUDIES

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RESEARCH AND TECHNOLOGY DEPARTMENT

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This is the first annual technical report of progress toward a crosstie random access memory. This marks a recent change in direction from the previously studied serial access memory. The more pertinent information learned from the serial memory approach which applies to the CRAM is repeated here. However, previous reports contain much additional important information and can be obtained by writing to the authors.

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It was realized at NSWC ~~in February 1981~~ that the crosstie memory elements could be reorganized into a random access memory and that this approach would eliminate some propagation problems which resisted easy resolution. At the same time, a much higher performance memory would result with higher expected reliability. Consequently, efforts at NSWC are being concentrated on the CRAM.

The expected characteristics of the CRAM are as follows: nonvolatile, non-destructive readout, ∿100 nsec read, ∿100 nsec write, very low power, wide temperature range (-50°C to 150°C), radiation resistant, high bit density ($3x10^5$ to $3x10^6$ bits/cm^2), low cost, standard supply voltages, no permanent magnets or keepers, no refreshing, and high bit to gate ratio.

It has been determined through previous work that permalloy can be deposited on the silicon dioxide layer of silicon wafers after the transistors are diffused. The following insulator and lead levels can be fabricated without damage to the permalloy. The CRAM is intended to be so integrated with the manufacture of integrated circuits. The permalloy itself can be used as a conductor although it is thin (∿350A). The subsequent conductor layers used for interconnection on the IC can most likely serve as the conductors for the CRAM also. Thus, by folding in the fabrication of the magnetic memory with conventional IC fabrication steps, the extra levels needed can be held to perhaps two.

Initial testing can be done, however, without fabrication of the integrated circuit which will eventually do the decoding, driving, and perhaps the amplification. Thus it is expected that in the near future, testing will be done on partially populated memories so a realistic notion of memory behavior can be obtained without the need of connecting to every row and column of the memory matrix.

FOREWORD

This report is intended to serve as an annual report to the Naval Air Systems Command. The work reported here was funded by AIRTASK A03A360F/009B/0F62-582-000 (FY80) and AIRTASK A03A360F/009B/1F62-582-000 (FY81).

The authors wish to acknowledge the help of Emma Lee Tull and ENS Scott Grundmeier, USN. They also thank Robert Reams of Harry Diamond Laboratories for his help in the use of the CAD facility and mask generator at that laboratory.

Ira M Blatstein

IRA BLATSTEIN
By direction

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ILLUSTRATIONS

CHAPTER 1

INTRODUCTION

As presently conceived, the Crosstie Random Access Memory (CRAM) will require five depositions and five masks. The first level will be anisotropic permalloy, followed by an insulator of silicon nitride or silicon monoxide. These levels will be followed by a layer of 95% aluminum - 5% copper, another insulator, and a final Al-Cu layer. All conducting layers will be chemically etched or ion milled, and the insulators will have vias opened using a liftoff procedure. All these procedures can be folded into the fabrication steps taken in the manufacture of integrated circuits. It is expected that the decoding and driving of the memory will be done by circuits on the same chip just as is done in semiconductor memories. The amplifier may also be integrated on the same chip but this has not been determined at this time.

By testing partially populated memories, a realistic idea can be obtained on drive levels, amplifier needs, and so forth. In the near future it is expected that several sizes of memory will be tested but only about eight rows and eight columns will be connected to external circuitry. This will provide 64 test bits in, for example, a 4K or 16K memory. At NSWC, efforts will be made to use conventional TTL circuits and video amplifiers. This will aid in defining integration requirements. Standard supply voltages will be used.

CHAPTER II

THE WIGGLE PATTERN

Anisotropic permalloy[1] films ~ 370Å thick, with Hk ~ 3.5 Oe and Hc ~ 1 Oe are used. The films are made in an ion beam coater. Conventionally deposited films can also be used. Isotropic films could be used but in our system it is easier to deposit anisotropic films. It is also easier to measure anisotropic films on our equipment. An 81-19 permalloy target is used in the ion beam coater. Care is taken to insure that the ions are arriving perpendicular to the plane of the substrate to avoid angle of incidence effects. The substrate is not heated but rises during film deposition to about 70°C. The deposition rate is about 10Å/sec using argon in the gun. The films vary at times from being a little iron rich to being slightly nickel rich for zero magnetostriction using this target. A magnetic field is present at the substrate during deposition to produce a well-defined easy axis. The target has to be rotated occasionally to avoid anisotropic target etching which causes the beam of Ni-Fe atoms to split into two concentrated beams. This causes uneven coverage on the substrate.

The permalloy film is then etched into a wiggle pattern as shown in Figure 1. Notice the direction of the easy axis in Figure 1. Next a 50 Oe magnetic field is applied (up in Figure 1). Then the magnetic field is turned off. Néel walls appear as shown in Figure 1 starting at one apex and terminating at the opposite apex. If no reverse field is applied, only positive Néel walls appear.

Some wiggle patterns are shown in Figure 2. The walls are made visible through the use of Bitter solution. In Figure 2(a), some cells contain zeros and some contain ones. In Figure 2(b), a modified version of the wiggle is shown with all zeros. All ones are shown in Figure 2(c). The preferred pattern at this writing is the pattern shown in Figures 2(b) and 2(c). A 10 Oe uniform field is needed to annihilate the crossties (up in Figure 2(c)). A 4 Oe field (down in Figure 2(b)) will nucleate crosstie-Bloch line pairs. Crossties do not form on the positive Néel walls in the narrow section to the right in Figure 2(c). This wall is only a 90° wall, and crossties form only in walls which have a rotation close to 180°.

The pattern shown in the last two photos of Figure 2 allows for a meandering column address line which always crosses the memory cell in the same direction. This makes it possible to address each bit by activating only two lines -- one a column address line and the other a row address line. This simplifies the logic compared to the scheme needed for Figure 2(a), but the density may suffer somewhat.

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[1] Cohen, M. S., "Ferromagnetic Properties of Films," in Handbook of Thin Film Technology, edited by L. I. Maissel and R. Glang (New York, McGraw Hill Book Co., 1970), pp. 17-1 to 17-88.

It is helpful to review crosstie behavior in unetched films. The static (very slowly changing) field required to generate a crosstie in a film depends on film thickness.[2] This is shown in Figure 3. At a given thickness, the amplitude of the generation and annihilation fields increases with decreasing pulse width. Curves shown in Figure 4 show[3] how large a field is needed for crosstie generation as a function of pulse length and film thickness in an unetched film. The field amplitude required for a 200 nsec pulse is about the same as the field required in the static case. From Figure 4 it is obvious that a 1 can be written in as short a time as 1 nsec if sufficient amplitude is used. Very little extra amplitude compared to the static case is needed to write a 1 in 50 nsec. The fields required to generate crossties in etched films increase with decreasing cell size. This is not a major limitation since for the same current the magnetic field increases with smaller conductor widths.

The time required to write a 0 if a 1 was present at that location is not the same as the time required to write a 1. The time it takes to annihilate a crosstie-Bloch line pair is dependent on the mobility of the Bloch line and the distance it is away from its neighboring crosstie. A 3 Oe field applied for 7 nsec will annihilate all periodic crosstie 5 μm apart in an unetched film.[4] But a 2 Oe pulse must persist for a longer time, perhaps 30 nsec, for annihilation. As the Bloch line approaches the crosstie, a repulsive force retards the Bloch line. A 1 Oe field is less than the annihilation field so it can be applied indefinitely. It will move the Bloch line close[5] to the crosstie, but not close enough for annihilation. Because of magnetostatic effects, larger fields are needed in etched films. These shape effects cause the equivalent of an anisotropy field in isotropic films, making their use possible. It is possible to vary the distance of a Bloch line from its neighboring crosstie by changing the shape of the wiggle pattern. The crosstie forms at the inside apex of the pattern.

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[2] Schwee, L. J., "Stability Conditions for Néel Walls and Crosstie Walls in Thin Magnetic Films," AIP Conf. Proc. 10, p. 996, 1972.

[3] Sery, R. S., "Dynamic Crosstie Nucleation Thresholds for Crosstie Memory," IEEE Trans. on Magn. MAG-11, No. 1, p. 29, 1975.

[4] Schwee, L. J. et al., "Progress Toward the Crosstie Memory," NOLTR 73-185, 1 Oct 1973.

[5] Middelhoek, S., "Ferromagnetic Domains in Thin Ni-Fe Films," Ph.D. Dissertation, University of Amsterdam, 1961.

CHAPTER III

WRITING

The field required to write at a particular location in the matrix must be applied using coincident currents. Two schemes for accomplishing this are described here. The scheme needed for the pattern of Figure 2(a) is shown in Figure 5 for writing a 1. (The wiggle pattern is shown without detail.) With the current direction shown for the meander line, current must be applied to every even row except for the row where a 1 is to be written. If a 1 is to be written on an odd row, current is reversed in the column address line, and current is applied along all odd row lines except on the row on which a 1 is to be written. The row lines must turn on before or nearly at the same time as the column lines or a 1 will be written on every other row along the activated column. In the figure, values for annihilation and generation were used for an unetched film. The values will be larger in an etched film depending on the dimensions used. Good margins of operation can be expected as shown in the figure. The number of row lines that must be turned on will be limited to 31 or 63 because of the readout method discussed in a later chapter. The logic to do this is straightforward and is discussed in a later chapter.

Using the same row conductors and meandering column conductors, a 0 can be written at any location. This is shown in Figure 6. For the current sense shown in the figure, all odd rows are activated plus the even row desired. To write on an odd row, the odd row plus all even rows are activated, and the current is reversed in the meander line. Again the logic to perform this is shown in a later chapter.

The row conductors will be on the first conductor layer above the permalloy film. This location is necessary so contact can be made to the amplifier from each wiggle for readout as will be seen later. The column lines will be on the last conducting layer.

A simpler write scheme is possible using the pattern shown in Figure 2(b and c). Here the meander line can be arranged to cross the memory cell always in the same direction. Then only one row need be activated to write at an arbitrary cell. Suppose that the crossties generate between -4 and -4.8 Oe. (Properly designed patterns can reduce the range of field over which generation may or may not occur compared to the average generation field.) Now suppose a negative field of 3 Oe is produced by the row conductor and the column conductor. Where these intersect, a 6 Oe field is present, and a 1 is written. Both currents could be off by $\pm$ 20% and it will still work.

This second arrangement is clearly more simple from a logic viewpoint, and consumes less power than the first scheme described.

The capacity between the activated column and all the activated rows amounts to less than a picofarad for anticipated drive line widths. As we have shown, 50 nsec is a sufficient time duration for writing a 1 and a 0. However, time is required for propagation delays through the decoders and logic. This will add another 30 nsec or so. Consequently, the write time, measured from the time the address is sent until writing is complete, should take approximately 100 nsec.

The magnetic field produced by a conductor in such a circumstance is given by the following equation,

$$H = (I/5S)\left\{\tan^{-1}[(b+S/2)/R]-\tan^{-1}[(b-S/2)/R]\right\} \qquad (1)$$

where I is current in amperes, S is the strip width, R is the insulator thickness, and b is the distance from the center of the strip at the permalloy film, with S, R, and b measured in centimeters. For a conductor 6 microns wide and 1000Å away from the film, the field produced by 1 ma is 1 Oe directly beneath the center of the strip.

CHAPTER IV

READING

The readout method described here uses the magnetoresistance[6] effect in the permalloy film. The effect can be described by the following equation

$$R = Ro + \Delta R/2 \cos 2\theta \qquad (2)$$

where ΔR is about 3% of the resistance of Ro, and θ is the small angle between the magnetization direction and the direction of current flow. The resistance Ro in permalloy films 370A thick is about 6Ω/square.

If we refer to Figure 7, four situations are illustrated showing the direction of magnetization for a memory cell containing a 0 with no external field, a 0 with a local field about 60% of the annihilation field applied, and also the magnetization directions for a 1 with and without the magnetic field. The local field described here is applied using the same row conductors described in the previous chapter on writing.

Now suppose a current is flowing through this column of the wiggle pattern. The current will flow approximately along the lines of magnetization shown in the 0 cases in Figure 7. Therefore we can expect that the angle θ of Equation 2 will be about zero for the case where a 0 is present with or without the local magnetic field. Little change in resistance is expected when a pulsed field is applied.

However, in the case of a 1 at zero applied field, the current encounters some magnetization at about 90° from its own direction. This happens where the current is most concentrated because of the sharp bend. In this case, lowered resistance exists. When the local field is applied, the Bloch line moves to the crosstie and the magnetization once again aligns itself approximately along the direction of current flow which is a high resistance situation. Because of Bloch line mobility and the repulsive force between the crosstie and Bloch line, a response time of about 20 nsec is anticipated. The pulse due to the change in resistance is expected to appear as shown in Figure 7, presuming that the applied field was a 20 nsec pulse.

One can estimate the resistance change between the 1 with no field applied and the 1 with a field applied by using the following considerations. Most of the current will take the short path around the bend. Here the angle θ is about 90°. This is what we want for a large signal. The bad part is the fact that the path is short, and consequently the resistance is low. We know that the resistance in the

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[6] McGuire, T. R. and Potter, R. I., "Anisotropic Magnetoresistance in Ferromagnetic 3d Alloys," IEEE Trans. on Magn. MAG-11, No. 4, p. 1018, 1975.

permalloy film is about 6Ω/square, but when the current goes around a 90° corner, the resistance is less than that. We can guess that the resistance affected by the crosstie is about .6 x 6Ω. Now we can split the current into two paths, one which is not affected by the crosstie-Bloch line pair and one which is. The longer path is about three times longer than the shorter path and in parallel to it. So we can write for the case where the field is applied if the resistance of the shorter path is r,

$$\frac{1}{R_f} = \frac{1}{r} + \frac{1}{3r} \quad \text{where } R_f = .6 \times 6\Omega. \tag{3}$$

When a field is not applied, the shorter path has 3% less resistance so we can write

$$\frac{1}{Ro} = \frac{1}{.97r} + \frac{1}{3r} . \tag{4}$$

The change in resistance when the field is applied is then

$$R_f - Ro = 3.6\Omega - 3.518\Omega = .08\Omega. \tag{5}$$

This rough estimate is good enough to guess at the amount of sophistication needed in the readout scheme. The signal is in the form of a resistance change, and resistors are easy to deal with.

The readout scheme prefered at this writing is shown in Figure 8. Here all wiggles are connected to one input of a differential video amplifier except for one wiggle which is used for reference. On the reference wiggle, no ones will ever be written. Once the address is sent, a single permalloy column and a single row conductor will be selected. In Figure 8, row 13, column 5 are selected for illustration. All other columns are disconnected using tri-state circuits. A pulse ∿ 20 nsec long is sent through the selected row conductor. If a 0 is present at row 13, column 5, then an identical signal will be received at both inputs to the amplifier and since the amplifier has a differential input, no signal is received from the amplifier. If, however, a 1 is present at row 13, column 5, the difference between a 0 and 1 is received from the amplifier. After amplification of 100 to 400 times, there is sufficient amplitude to trigger a bidirectional one shot with a comparator input. This will bring the output signal up to TTL levels.

The purpose of the dummy reference column is to eliminate or reduce common mode signals and to decrease time required for the amplifier to settle down once a row and column are selected. Also the reference column eliminates amplifier output if a 0 is being detected. This simplifies later decision making with a one shot or with a comparator with hysteresis.

The resistance in each magnetoresistor would be 1000Ω or so if a 5 ma current is used through the wiggle pattern. This allows for about 64 bits vertically in each magnetoresistor.

In this arrangement the signal due to a 1 can be easily calculated. One of the magnetoresistors will change from 999.92Ω (using the 0.08Ω value of Equation 5) to 1000Ω when the field is applied. The amplifier sees a change of 200 μv. The input impedance to the amplifier is 500Ω. Because of the nature of the expected

signal, the amplifier can be narrow-banded to pass frequencies between about 25 MHz and 50 MHz or perhaps a narrower band would do. With a 25 MHz bandwidth and an input impedance of 500Ω, the thermal noise at the input will be

$$V_h = \sqrt{4kTR\Delta f} = 14\ \mu v \qquad (6)$$

which gives a signal to noise ratio of 14.

An important factor here may be to use if possible a frequency band which excludes switching frequencies. Using TTL, the risetimes on pulses can be about 5 nsec and a slightly higher frequency pass band would be needed to pass these. The pulse used to tickle the wiggle for example could cause an unwanted spike on the amplifier output. Such a spike may well be too fast to trigger a one shot however.

A thin film circuit similar to that shown in Figure 8 with various different wiggle patterns has been designed and masks have been generated, but it has not yet been fabricated. It will be used to find prefered wiggle patterns and test the readout technique.

In the meantime, an amplifier has been wired together to test the readout. The amplifier circuit is shown in Figure 9. The 592 or 733 video amplifier was found to work very well in this application. It has excellent common mode rejection and can be easily converted to a high pass amplifier by placing a capacitor across the gain select pins. To test the amplifier, the two 10 megohm resistors were connected to a TTL oscillator and driven from nearly 0 to nearly 5 volts in bursts. This provided a 250 μv signal at each amplifier input. To simulate a 1, two capacitors (shown by dotted lines in Figure 9) were used to slow down the response time at one input, thus simulating the response of the Bloch line. A small cheating capacitor across the amplifier inputs was found to be helpful in reducing unwanted feedthrough from the TTL oscillator without interfering with the signal. Such a capacitor can be very helpful in reducing high impedance pickup due to ground currents radiation, etc. The amplifier with a gain of 100 was followed by a 760 high-speed comparator with hysteresis which brought the output up to TTL levels. A one shot with a comparator input such as the Signetics 8T20 would probably be better in this application. Such a one shot could trigger off the low to high voltage swing and reset itself without the need for a high to low voltage swing. The trigger level must be set above the noise level in this case also. The circuit described above worked very well, but may well need some modification when the real output is tested.

If it is found that the readout method described above does not have a sufficiently low error rate, a pulse train can be used. Then the amplifier can be narrow-banded further, and coherent integration can be used. This would extend the readout time to perhaps a microsecond.

The amplifier and comparator described above have propagation delays of about 25 nsec combined, and it is anticipated that some settling time will be required after a particular column is selected by the address. Also about 30 nsec will be needed for the logic to select a particular line. The access time should be somewhere between 100 and 200 nsec if one tickle pulse is used. The video amplifier and the comparator together cost about two dollars.

Instead of using 128 bits and about 5 ma in each column, 64 bits and about 10 ma could be used. This would both double the output signal and decrease the amplifier input impedance to 250Ω. It would also reduce the number of row conductors which must be turned on for writing to about 32 if that scheme is used. The limitation on the current used is dependent on how often a column is successively addressed and the duty cycle.

The power supplies on the video amplifier and comparator could be reduced to ± 5 volts if desired.

CHAPTER V

CIRCUIT DIAGRAM FOR SIXTEEN BITS

It has been presumed from the beginning that the CRAM will be integrated on a chip with decoding circuitry. The density is about right for this. All drive levels are easily within range of conventional TTL circuitry. The best way to lay out the logic and such questions are not being addressed at this time. First the memory must be tested using various densities and drive levels must be determined. However, the logic required for a sixteen-bit memory was considered for the more complicated write scheme and is shown in Figure 10. Here a phase sensitive detection scheme was outlined instead of the method described in the previous chapter.

The number of logic functions per row and column averages to four not counting the decoders. If we consider an n by n matrix, the number of gates beyond the decoders would be 8n. But the number of bits is n^2. So the number of bits/gate is n/8. The larger the memory, the more bits/gate. The fact that the number of transistors required goes as n rather than n^2 suggests that rather large memories ought to be possible with good yields compared to semiconductor memories.

One of the immediate objectives of the CRAM program at NSWC is to fabricate a 4K memory but only connect to 4 to 8 rows and 4 to 8 columns. This will allow testing of 16 to 64 bits to determine optimum drive levels and identify what problems may arise from parasities, high frequency feedthrough, ground currents, etc.

A concrete goal is the pin for pin replacement of a popular dynamic RAM. Such a device could be retrofitted into several present systems. The very low power requirements of the CRAM will allow for much more dense packaging or, in other words, a large increase of memory in the same volume.

CHAPTER VI

EXPECTED CHARACTERISTICS VS. PRESENT COMPETITION

The expected characteristics of the CRAM are as follows:

nonvolatile

random access

non-destructive readout

$\sim$ 100 nsec write

$\sim$ 100 nsec read

high bit density ($3x10^5$ to $3x10^6$ bits/cm^2)

very low power

wide temperature range (-50°C to +150°C)

radiation resistant

low cost

standard voltages

no permanent magnets or moving parts

no standby power needed

no refreshing needed

high bit to gate ratio.

The CRAM will require magnetic shielding, but this is a simple task since no external fields are required.

It is, of course, very difficult to clearly foresee all problems which may arise in the development of the CRAM. It is also difficult to estimate costs. However, by comparing the CRAM to other technologies, some guesses can be made. This is done in Figure 11. Here we allowed ourselves a large range of access times and a large variation in cost. Data on the other technologies is taken from an IEEE Spectrum article in March 1981 by Choo S. Chi. The reason the CRAM can be

expected to be cheaper than the dynamic RAM is that fewer transistors are needed, and no refreshing is needed. If this is not enough to make it cheaper on a chip level, it should on a system level where refreshing can present many difficulties. Even if the CRAM costs 10 times more than expected, it will be a memory of choice because of its light weight, low power, and small volume compared to core. The access time was drawn up to a microsecond in case a pulse train is needed for detection.

From Figure 11 it becomes apparent that there is not much competition for the CRAM. It appears to be at least ten times faster or ten times cheaper than any close nonvolatile competitor and has many other advantages besides. It also appears that development will be straightforward without the need for material research.

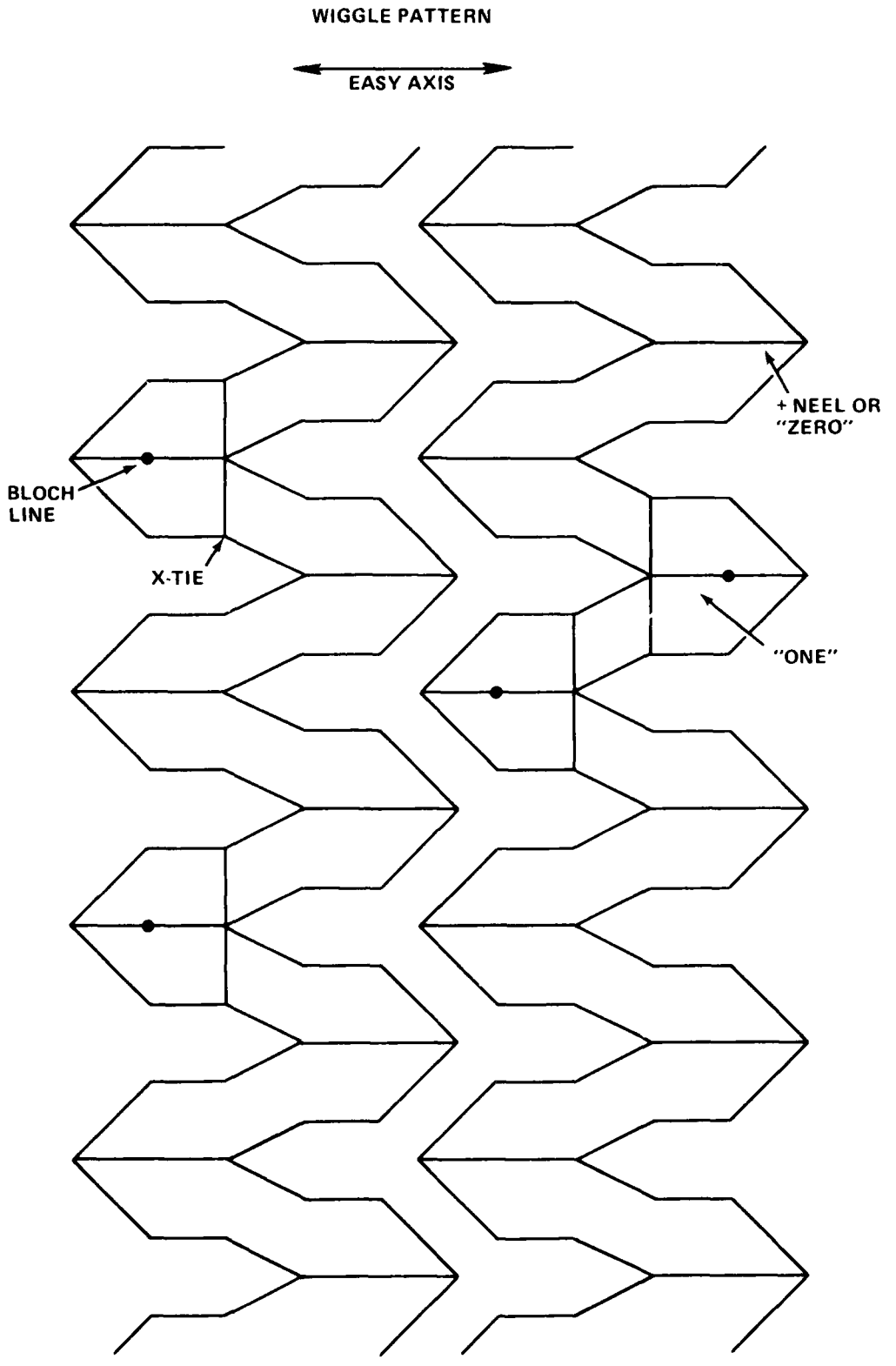

FIGURE 1 CROSSTIE-BLOCH LINE PAIRS STORED IN WIGGLE PATTERN

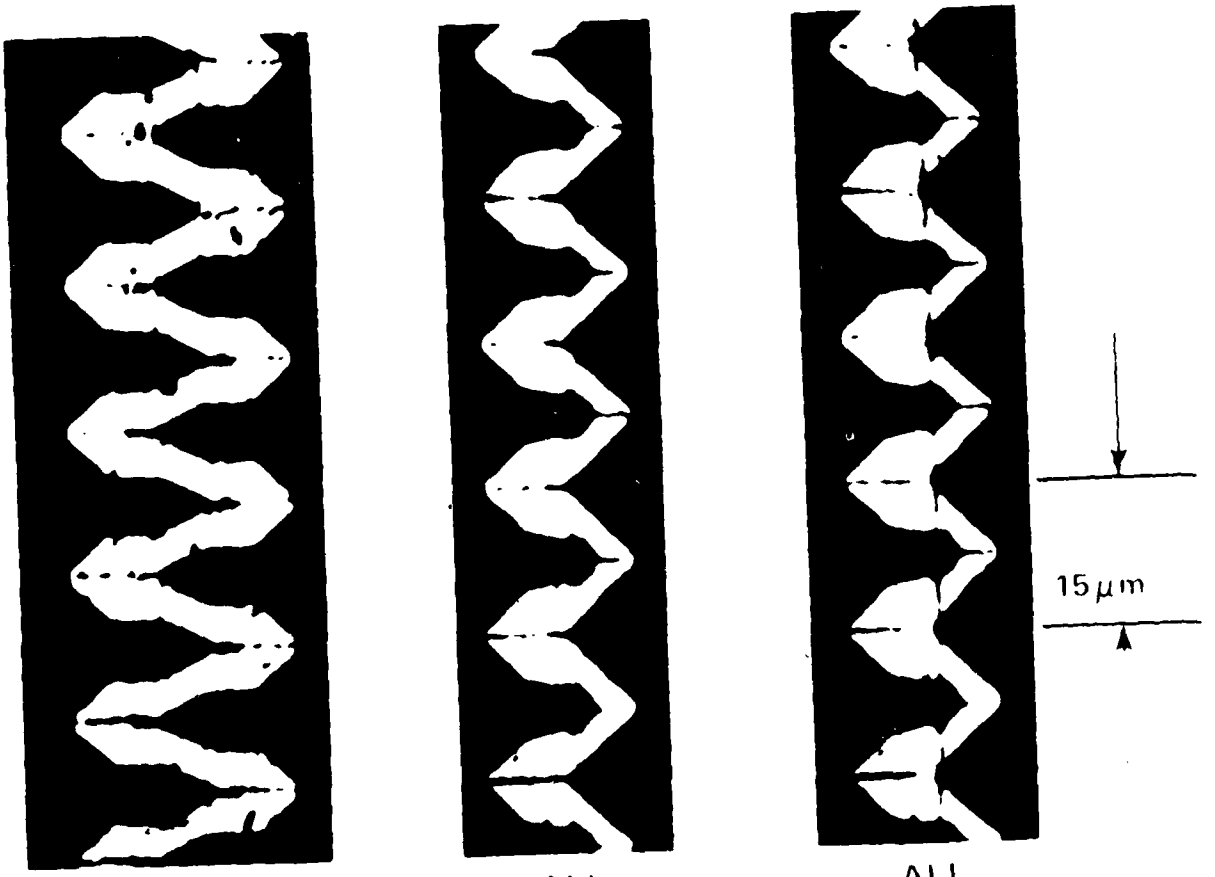

FIGURE 2 BITTER SOLUTION SHOWING WALLS IN WIGGLE PATTERNS

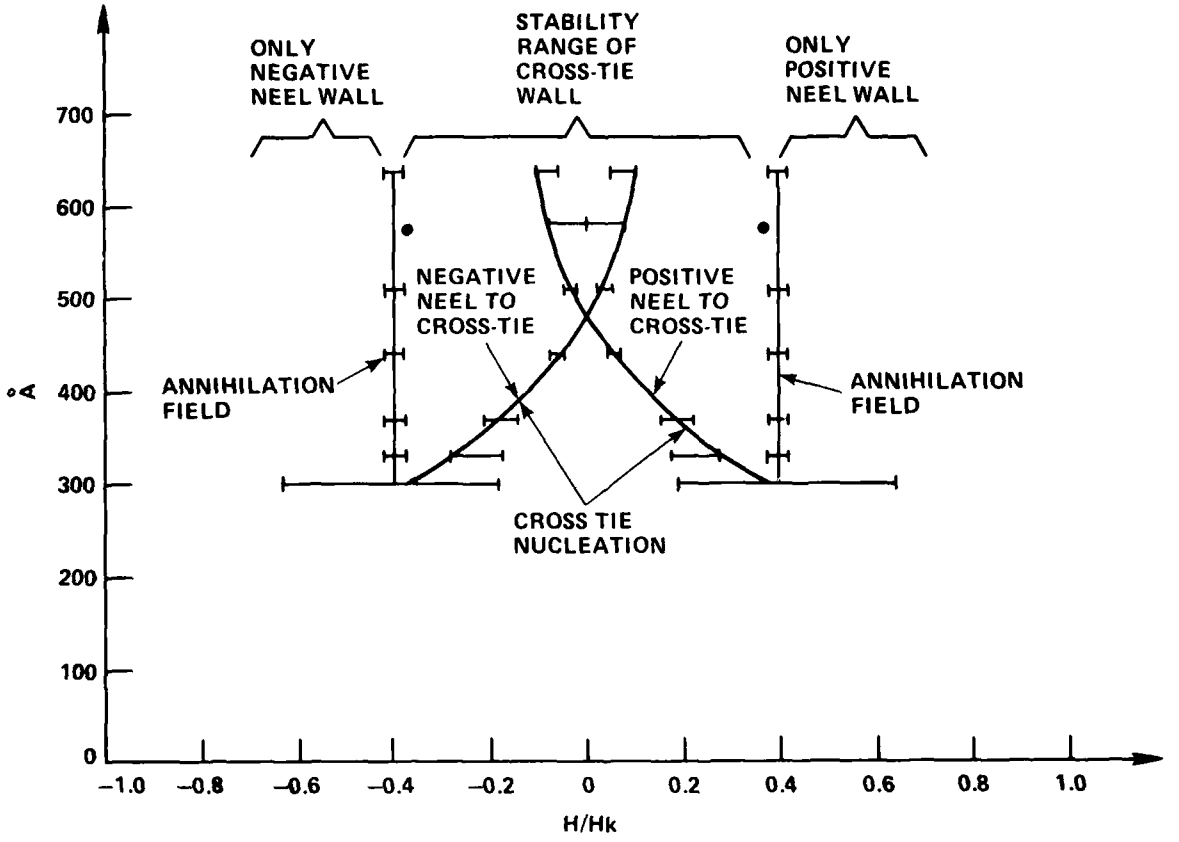

FIGURE 3 GENERATION AND ANNIHILATION FIELDS AS A FUNCTION OF FILM THICKNESS

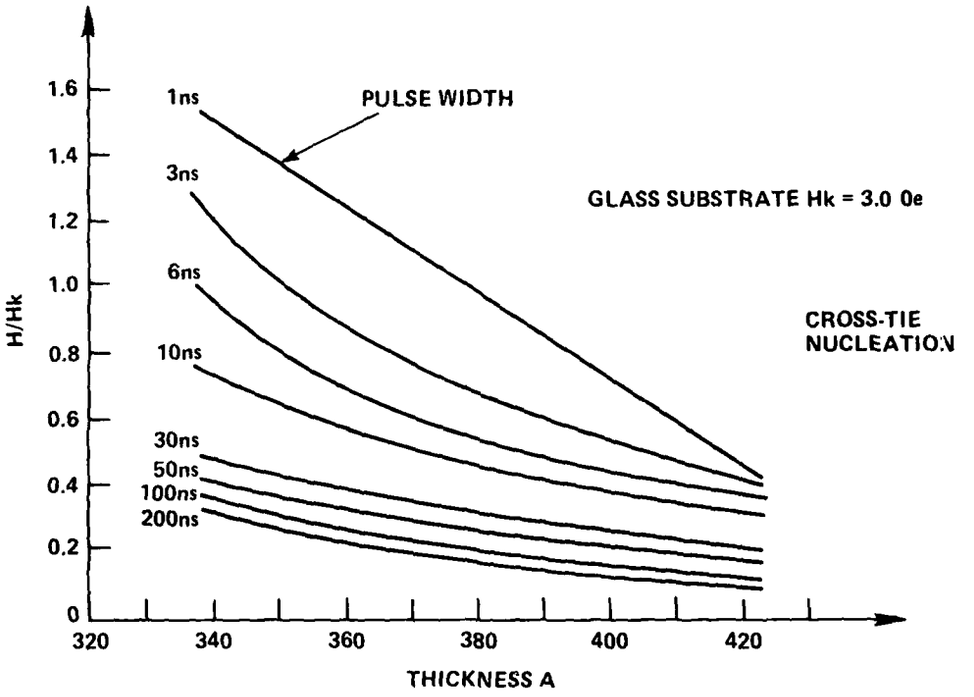

FIGURE 4 FIELDS REQUIRED TO GENERATE A CROSSTIE-BLOCH LINE PAIR AS A FUNCTION OF PULSE WIDTH

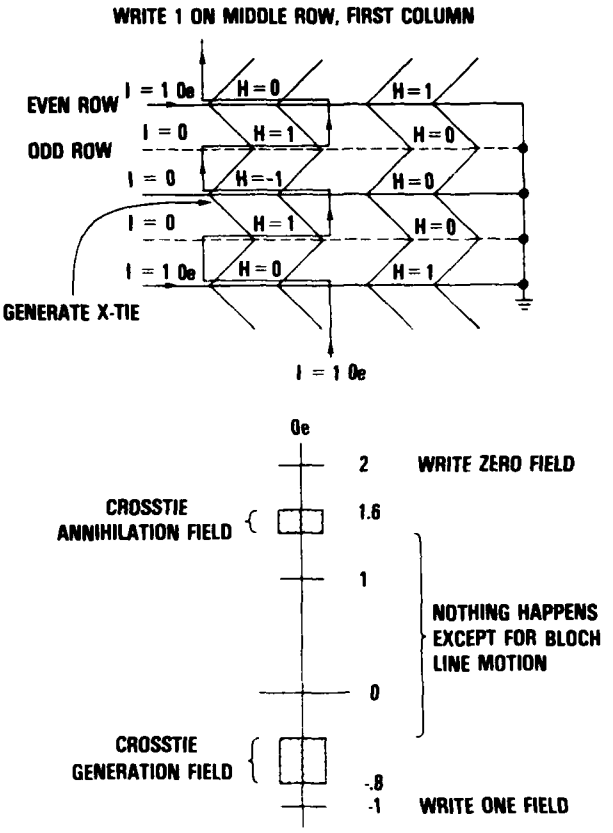

FIGURE 5 WRITE "ONE" SCHEME WITH DRIVE FIELDS NORMALIZED TO AN UNETCHED FILM

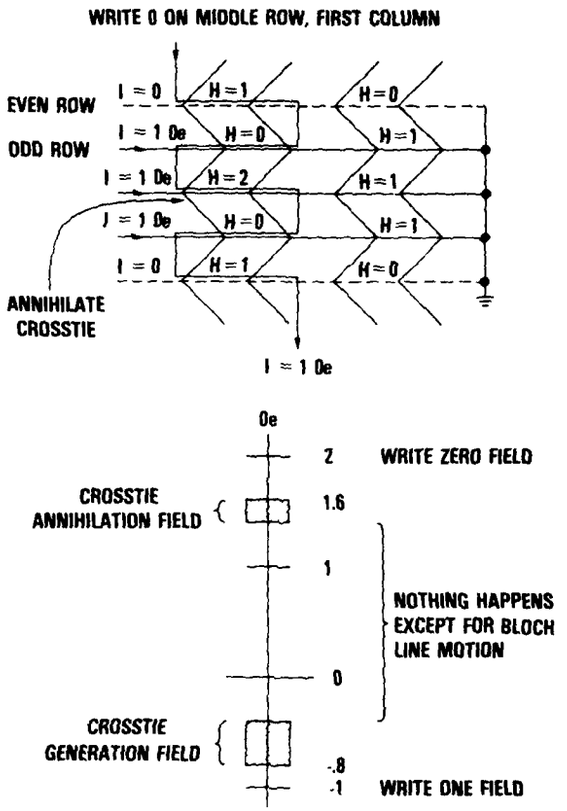

FIGURE 6 WRITE "ZERO" SCHEME WITH DRIVE FIELDS NORMALIZED TO AN UNETCHED FILM

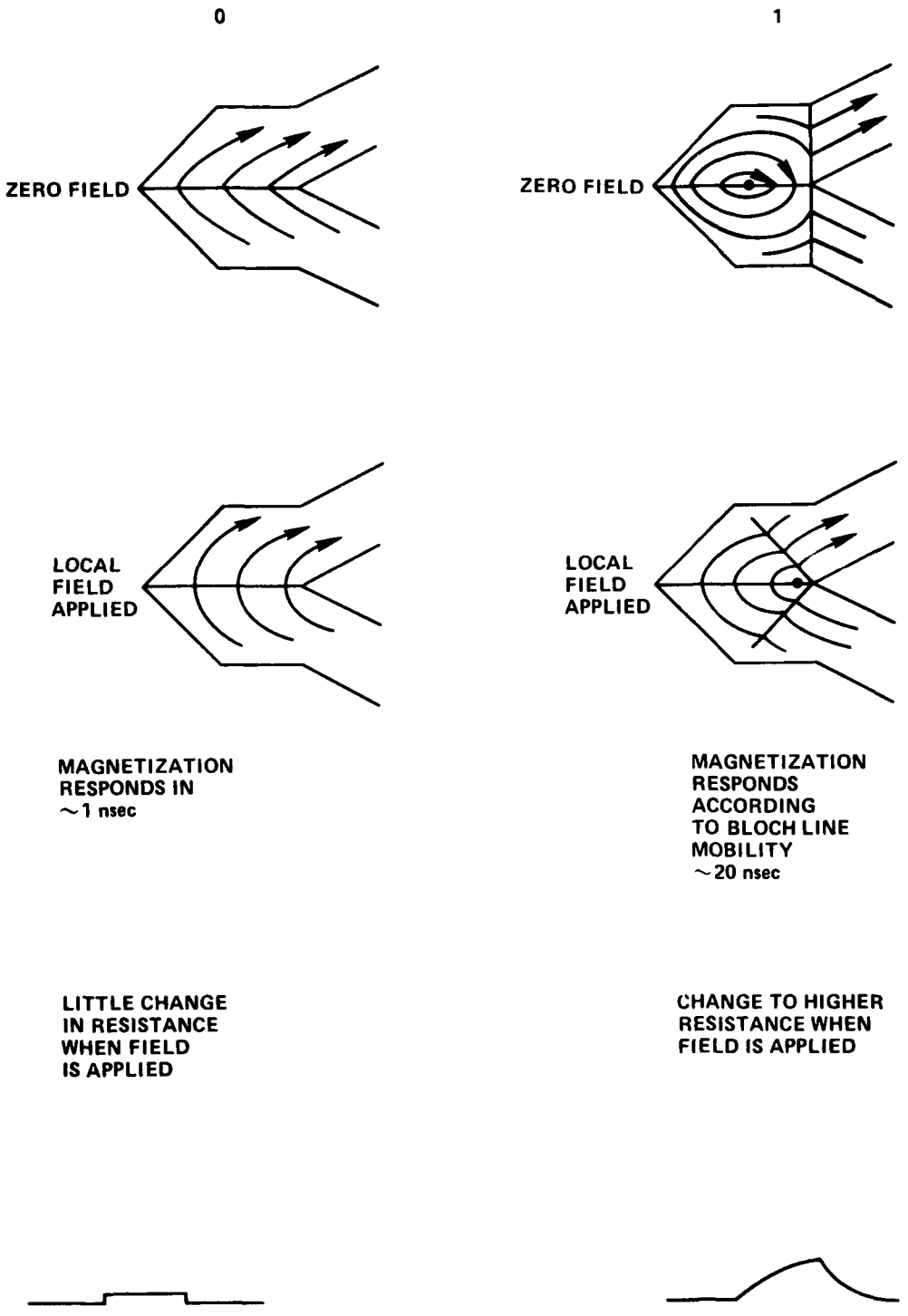

FIGURE 7 MAGNETIZATION DIRECTIONS FOR 0 AND 1 WITH AND WITHOUT A LOCALLY APPLIED FIELD

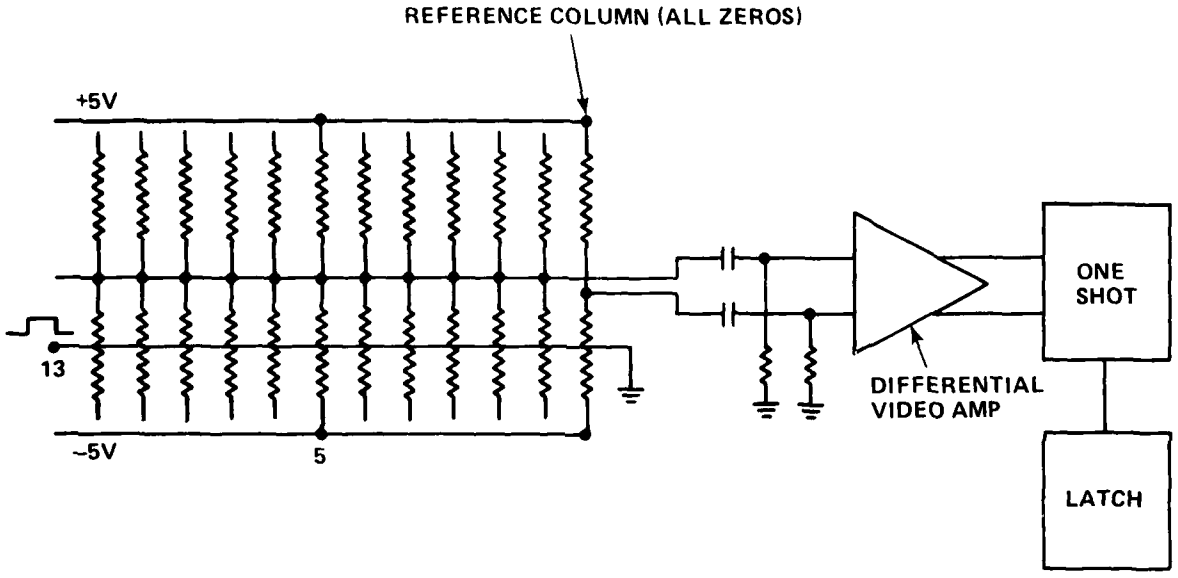

FIGURE 8 READOUT METHOD USING A REFERENCE COLUMN, A SELECTED COLUMN, AND A TICKLE FIELD

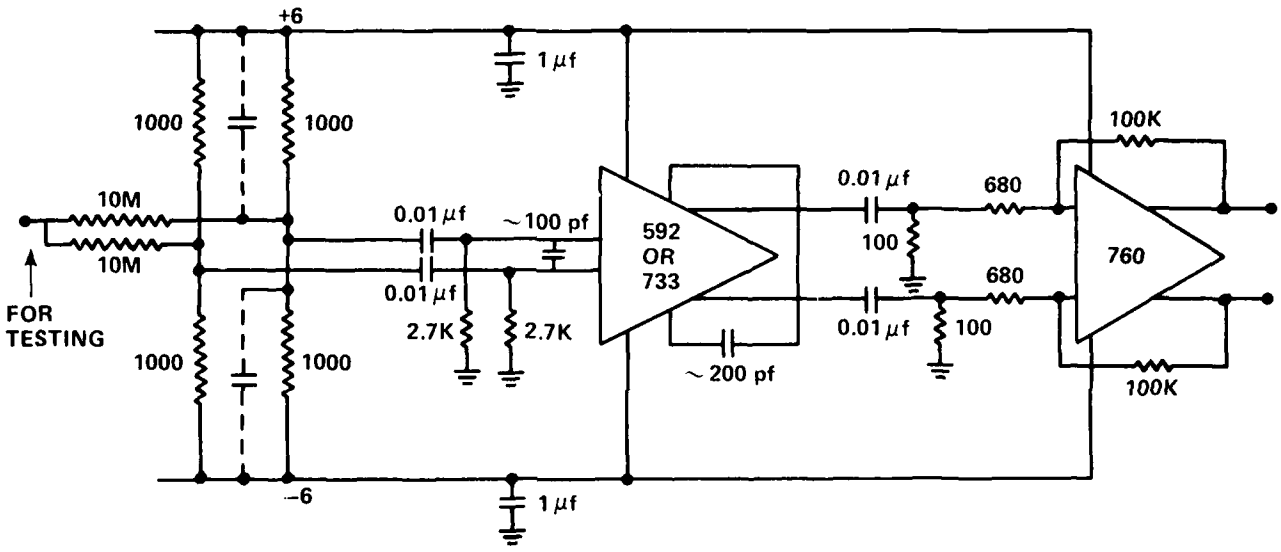

FIGURE 9 READOUT AMPLIFIER CIRCUIT AND COMPARATOR WITH HYSTERESIS

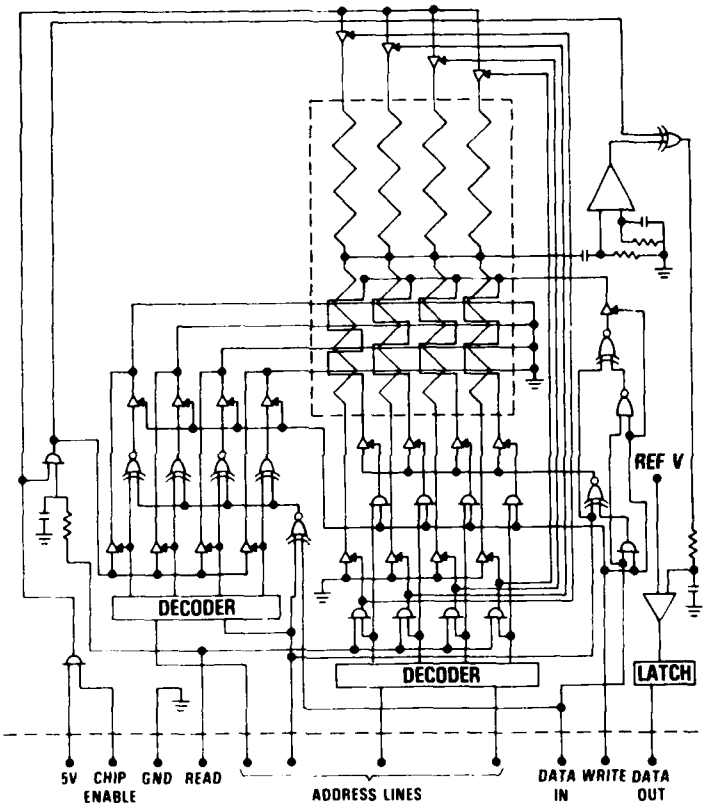

FIGURE 10 LOGIC REQUIRED FOR A SIXTEEN BIT MEMORY

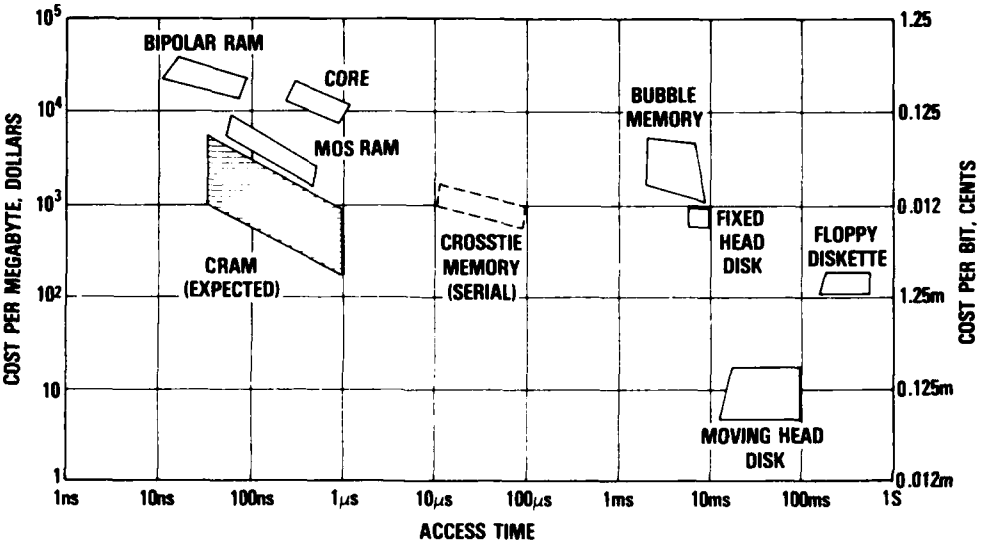

FIGURE 11 PERFORMANCE VS COST OF PRESENT TECHNOLOGIES AND THE CRAM

APPENDIX A

A NEW METHOD OF LOCKING A DOMAIN WALL

Before the switch was made to the CRAM, some experiments were done to find an alternate approach to propagation. It was our desire to find a way to trap a wall so it could not easily be moved, provide potential wells along the wall so crosstie and Bloch lines would naturally position themselves, and increase the possible density of the serial memory to about four million bits/in^2. In addition, we wished to be able to propagate the crosstie-Bloch line pairs using only one conductor layer. To accomplish all these goals simultaneously, the film shown in Figure 12 was fabricated. The film was grown to a thickness of 630Å. Then it was protected with photoresist in the oval shaped regions. Then it was ion milled to a thickness of about 370Å. As a consequence, the film shown in Figure A-1 is 370Å thick except on the oval plateaus where it is 630Å thick. After a field is applied (up in Figure A-1), a Néel wall appears caught between the rows of oval plateaus. The lowest wall shown in the picture is a return wall of a domain formed by the lower row of plateaus. The wall is trapped because the film is thin compared to the plateaus, and therefore the wall has less energy. A 2 Oe field was needed along the easy axis (left to right in the photo) to dislodge the wall.

When a negative field was applied, crossties formed in predictable locations on the trapped wall as shown in Figure A-2. The asymmetrical pattern was used so a conductor placed above each row of plateaus could produce the proper fields to propagate the crosstie-Bloch line pairs. Thus, an alternative to the serrated strip method of propagation was found, but it has not been pursued.

A symmetrical pattern of oval plateaus was also generated as shown in Figure A-3. Here the crossties also have potential wells along the trapped wall. It was expected that the permalloy would later be removed outside the area of the oval rows perhaps using a serrated strip pattern. This would eliminate the return wall shown in each of the last three figures.

Such control over domain wall formation may prove to be useful in future devices. Domain walls need not be treated statistically and considered as Barkhausen noise generators. Indeed, in properly etched films, walls can become the signal generators in a new line of magnetometers, inductors, and other magnetic devices. The magnetoresistance effect is not very useful when domains are used in anisotropic films because of the cos 2θ law. However, when used with several trapped domain walls and Bloch line motion, large and useful signals can be generated.

FIGURE A-1 ION MILLED PATTERN USED TO TRAP A WALL

FIGURE A-2 CROSSTIES ON THE TRAPPED WALL

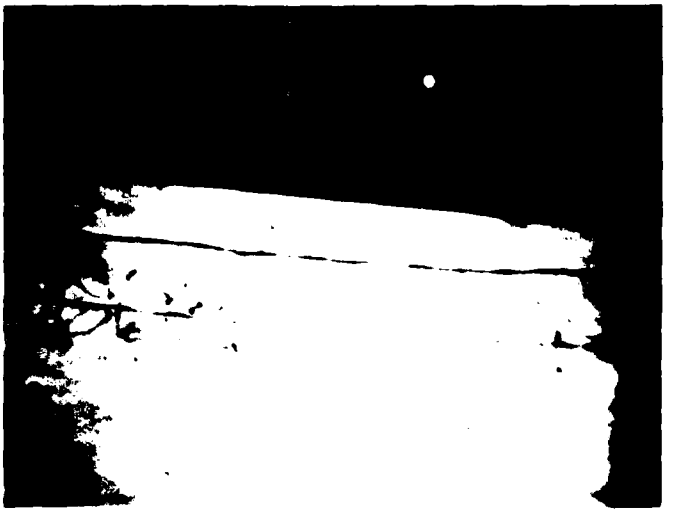

FIGURE A-3 A SYMMETRICAL PATTERN FOR TRAPPING A WALL

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